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METHODS OF MAKING THIN INTEGRATED CIRCUIT DEVICE PACAKGES WITH IMPROVED THERMAL PERFORMANCE AND INCREASED I/O DENSITY

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation-in-part of U.S. Application Serial No. 10/354,772 entitled INTEGRATED CIRCUIT DEVICE PACKAGES AND SUBSTRATES FOR MAKING THE PACKAGES filed January 30, 2003, which is a continuation of U.S. Application Serial No. 09/434,589 entitled INTEGRATED CIRCUIT DEVICE PACKAGESAND SUBSTRATES FOR MAKING THE PACKAGES filed November 5, 1999 and issued as U.S. Patent No. 6,580,159 on June 17, 2003, the disclosures of which are incorporated herein by reference.

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

[0002] Not Applicable

BACKGROUND OF THE INVENTION

[0003] The present invention relates generally to leadless plastic semiconductor packages and, more particularly, to multi-row QFN-style semiconductor package of improved thermal performance and increased I/O density.

[0004] There is currently known in the electronic arts plastic semiconductor packages referred to as a Quad Flat Non-Lead (QFN) package and a Plastic Quad No-Lead Staggered Multi-Row Package (QFP-N). The QFN and QFP-N semiconductor packages each typically include metallized terminals located at the bottom of the package body along its periphery in

one, two or three rows, the rows in the QFP-N package being arranged in a staggered fashion. By these designs, the terminals are essentially flush with the bottom surface of the plastic package body, the QFN and QFP-N packages thus being considered to be "leadless" or "no-lead" packages. As indicated above, these particular packages may have one, two or three rows of terminals on all four sides of the bottom surface of the package body, and may have either a square or rectangular body as well as symmetrical or non-symmetrical terminal patterns. The staggered terminal configuration in the QFP-N package allows for ease of leadframe fabrication, package assembly, testing and surface mounting.

[0005] One of the major drawbacks associated with currently known QFN and QFP-N semiconductor package products is the very high production cost associated with the multiple row design of such packages. In this regard, currently known fabrication processes for QFN and QFP-N packages typically involve a build-up technology that requires the completion of multiple etching steps and the plate-up of copper interconnects. The copper interconnects or "busses" are included as a result of the need to interconnect the leads or terminals of the semiconductor package for purposes of completing the necessary step of electrolytically plating layers of nickel and gold to each of the leads or terminals thereof. In addition to increasing cost, the inclusion of the busses compromises the ability to maximize the I/O density of the semiconductor package.

[0006] The present invention addresses the shortcomings of the prior art by providing a leadless plastic semiconductor package which utilizes either an etch-back process or direct immersion gold plating process in order to increase the input/output density of the package, and reduce the manufacturing costs associated therewith. The increased I/O density is accomplished as a result of the plating busses of the present semiconductor package either being removed or not required at all in the final design. This allows for the assembly of multiple-row QFN or QFP-N semiconductor packages in accordance with the present invention which may optionally include power and/or ground rings. These and other attributes and advantages of the present invention will be described in more detail below.

BRIEF SUMMARY OF THE INVENTION

[0007] In accordance with the present invention, there is provided a QFN or QFP-N semiconductor package that is fabricated through the implementation of either an etch-back process or direct immersion gold plating process. The implementation of either of these

processes effectively increases the input/output density of the package. The increased density is accomplished as a result of the plating busses of the package either being removed through the implementation of the etch-back process, or not required at all in the final design if the direct immersion gold plating process is implemented during the fabrication of the package. These particular processes allow for the assembly of multiple-row QFN or QFP-N packages which may optionally include power and/or ground rings in the multi-row designs.

[0008] In the semiconductor package of the present invention, two or three layer tape is used as the medium for the routing of the I/O's of the package. The use of the two layer or three layer tape and either etching off the plating busses after the completion of Ni/Au plating, or not having the plating busses in the first place as a result of using the electroless direct immersion gold plating process allows for a substantial increase in the I/O density of the resultant semiconductor package while at the same allowing a multiple row package to be produced at a cost which is substantially below that of similar packages which require the completion of multiple etching steps and the plate-up of copper interconnects during the fabrication process.

[0009] The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0011] Figure 1 is a cross-sectional view of a semiconductor package constructed in accordance with a first embodiment of the present invention;

[0012] Figure 2 is a bottom plan view of the semiconductor package shown in Figure1;

[0013] Figure 3 is a cross-sectional view of a semiconductor package constructed in accordance with a second embodiment of the present invention;

[0014] Figure 4 is a bottom plan view of the semiconductor package shown in Figure 3;

[0015] Figure 5 is a bottom plan view of a semiconductor package constructed in accordance with a third embodiment of the present invention; and

[0016] Figure 6 is a chart which provides the process flow steps for an electroless immersion gold plating process which may be implemented in relation to one embodiment of the present invention.

[0017] Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figures 1 and 2 depict a semiconductor package 10 constructed in accordance with a first embodiment of the present invention. The semiconductor package 10 has the structural attributes of a semiconductor package commonly referred to as a Quad Flat No-Lead (QFN) package. However, those of ordinary skill in the art will recognize that the various structural elements included in the semiconductor package 10 and the exemplary manufacturing process related thereto as will be described in more detail below are applicable to semiconductor packages having configurations different from that associated with a QFN package, e.g., a Plastic Quad No-Lead Staggered Multi-Row (QFP-N) package.

[0019] The semiconductor package 10 comprises a film layer 12 which defines opposed, generally planar top and bottom surfaces. The film layer 12 is a generally planar sheet which is fabricated from a non-conductive material. By way of example, the film layer 12 may be fabricated from a polyimide film. Alternatively, the film layer 12 may be formed of a fiber-reinforced epoxy laminate, woven aramid, BT laminate or other plastic material. Disposed within the film layer 12 are a plurality of openings 14 which extend between the top and bottom surfaces thereof. As shown in Figure 1, each of the openings 14 has a generally quadrangular (i.e., square) configuration. The openings 14 of the film layer 12 include a relatively large, generally square opening positioned in the approximate center of the film layer 12, and a series of smaller, generally square openings 14 which are arranged in an inner row which circumvents the central opening 14, and an outer row which circumvents the inner row. The openings 14 of the outer row extend to at least one of the peripheral edge segments of the film layer 12.

[0020] In addition to the film layer 12, the semiconductor package 10 includes a die pad 16 which itself defines opposed, generally planar top and bottom surfaces, and has a generally quadrangular (i.e., square) configuration. As seen in Figure 1, the peripheral portion of the top surface of the die pad 16 is attached to the bottom surface of the film layer 12 such that a substantial portion of the top surface of the die pad 16 is exposed within the central opening 14

of the film layer 12. The semiconductor package 10 also includes a plurality of leads 18 which each have a quadrangular configuration. Each lead 18 defines opposed, generally planar top and bottom surfaces. Additionally, the peripheral portion of the top surface of each lead 18 is attached to the bottom surface of the film layer 12 such that a substantial portion of the top surface of each lead 18 is exposed within a respective one of the openings 14 of the film layer 12 which are arranged in the inner and outer rows circumventing the central opening 14 (in which the die pad 16 is exposed). Thus, the leads 18 are themselves arranged in an inner row which circumvents the die pad 16, and an outer row which circumvents the inner row. As seen in Figure 2, the leads 18 of the outer row, like the openings 14 of the outer row, extend to at least one of the peripheral edge segments of the film layer 12. More particularly, those leads 18 (and openings 14) which are located at respective ones of the four corner regions defined by the film layer 12 extend to each of an adjacent pair of peripheral edge segments thereof.

[0021] The semiconductor package 10 further comprises an integrated circuit device or semiconductor die 20 which is attached to the portion of the top surface of the die pad 16 exposed within the central opening 14. The attachment of the semiconductor die 20 to the die pad 16 is preferably accomplished through the use of a layer 22 of a suitable adhesive. The contacts or terminals of the semiconductor die 20 are electrically connected to respective ones of the leads 18 through the use of elongate, conductive bond wires 24. More particularly, each wire 24 has a first end which is electrically connected to a respective one of the pads or terminals of the semiconductor die 20, and an opposed, distal end which is electrically connected to the portion of the top surface of a respective one of leads 18 which is exposed in a respective one of the openings 14 of the inner and outer rows thereof, as is shown in Figure 1.

[0022] In the semiconductor package 10, the semiconductor die 20, wires 24, the top surface of the film layer 12, and portions of the top surfaces of the die pad 16 and leads 18 which are exposed within the openings 14 are covered by a package body 26 of the semiconductor package 10. The package body 26 has a generally square configuration, and defines a generally planar top surface and four generally planar side surfaces. The bottom surface of the package body 26 is completely covered by the combination of the film layer 12, die pad 16, and leads 18. The package body 26 is typically fabricated from a plastic material (e.g., thermosets) via a molding process. In the completed semiconductor package 10, the bottom surfaces of the die pad 16 and leads 18 extend in generally co-planar relation to each other along a plane which is

generally parallel to and spaced outwardly from the plane defined by the bottom surface of the film layer 12. The leads 18 of the outer row each include an outer end which extends to and is substantially flush with a respective side surface of the package body 26. Though the openings 14 of the inner and outer rows of the leads 18 are each described as preferably having quadrangular configurations, those of ordinary skill in the art will recognize that each of these elements may alternatively have a circular or other configuration.

[0023] Having thus described the structural attributes of the semiconductor package 10 of the first embodiment, an exemplary method for fabricating the same will now be described. In the initial step of the fabrication method, an unpatterned, non-conductive sheet is provided which will eventually form the film layer 12. Thus, the non-conductive sheet is fabricated from the same material described above in relation to the film layer 12. An unpatterned metal layer (typically fabricated from copper) is attached to the sheet, the metal layer ultimately forming the die pad 16 and leads 18 of the semiconductor package 10 shown in Figure 1. The metal layer may be deposited on the non-conductive sheet using a sputtering or other metal deposition process. Alternatively, the metal layer may comprise a metal sheet which is mechanically attached to one side or face of the non-conductive sheet through the use of an adhesive.

[0024] Subsequent to the application of the unpatterned metal layer to the non-conductive sheet, the metal layer is patterned to facilitate the formation of the die pad 16 and leads 18. In addition to facilitating the formation of the die pad 16 and leads 18, the patterning process facilitates the formation of plating traces which are arranged so as to electrically interconnect the leads 18 and die pad 16. The plating traces are used in conjunction with an electrolytic plating process which will be described in more detail below. The patterning of the metal layer is preferably performed through the use of a conventional chemical etching process. In this process, a layer of photoresist is applied to the metal layer. The photorerist is exposed to light and developed, thereby forming a patterned mask of photoresist material on the metal layer. Next, a liquid etchant is applied, the etchant dissolving the metal that is not protected by the photoresist, thus transferring the photoresist mask pattern to the metal layer. Thereafter, the photoresist mask is removed. Subsequent to the patterning of the metal layer in a manner facilitating the formation of the die pad 16 and leads 18, the non-conductive sheet is patterened in a manner facilitating the formation of the openings 14 therein. The patterning of the non-conductive sheet to form the openings 14 may also be performed by a chemical etching process.

More particularly, where the sheet is a polyimide film, the patterning of the sheet is performed by chemically etching the same in a basic solution using a photoresist mask. The solution chosen to etch the non-conductive sheet should not etch the metal layer, with the solution chosen to etch the metal layer not etching the non-conductive sheet. Those of ordinary skill in the art will recognize that the etching or patterning of the non-conductive sheet may occur prior to the etching or patterning of the metal layer. As indicated above, the patterning of the non-conductive sheet facilitates the formation of the above-described film layer 12.

[0025] Subsequent to the "etch-back" of the metal layer and non-conductive sheet as facilitates the formation of the die pad 16, leads 18 and film layer 12, those portions of the top surfaces of the leads 18 which are exposed in respective ones of the openings 14 of the inner and outer rows are preferably plated. That portion of the top surface of the die pad 16 which is exposed within the central opening 14 of the film layer 12 may also be plated. A typical plating metal for copper is nickel/gold, which is used to enhance the connection of the bond wires 24 to the leads 18. Such plating is preferably completed through the implementation of a conventional electrolytic plating process. As will be recognized, if the exposed portion of the top surface of the die pad 16 is not to be plated, the plating trace that would otherwise extend thereto may be omitted in the patterning of the metal layer.

[0026] Subsequent to the completion of the plating process, a photoresist mask is applied to the bottom surfaces of the die pad 16 and leads 18, with a second chemical etching process being completed to facilitate the removal of the plating traces formed as a result of the initial etch or patterning of the metal layer. The plating traces, which extend along portions of the film layer 12 disposed between the leads 18 and die pad 16, are removed as a result of the implementation of the second chemical etching process, thus electrically isolating the leads 18 from the die pad 16 and from each other.

[0027] Upon the removal of the plating traces in the above-described manner, the semiconductor die 20 is attached to the exposed portion of the top surface of the die pad 16 through the use of the above-described adhesive layer 22. Thereafter, the conductive wires 24 are used to electrically connect respective ones of the pads or terminals included on the top surface of the semiconductor die 20 to respective ones of the leads 18. As will be recognized, the distal end of each wire 24 will be extended to the Ni Au plating layer included on each lead 18 within each opening 14 of the inner and outer rows thereof. Subsequent to the electrical

connection of the semiconductor die 20 to the leads 18 through the use of the wires 24, the die 20, wires 24, the top surface of the film layer 12, and portions of the top surfaces of the die pad 16 and leads 18 are covered by the package body 26 which, as indicated above, is typically formed via a molding process. The formation of the package body 26 completes the fabrication process associated with the semiconductor package 10.

[0028] Those of ordinary skill in the art will recognize that multiple semiconductor packages 10 may be assembled simultaneously by having a metal layer applied to a non-conductive sheet wherein the metal layer and non-conductive sheet are of sufficient size to allow for the patterning of multiple die pads 16 and corresponding inner and outer rows of leads 18 at the same time. Each die pad 16 and the leads 18 of the corresponding inner and outer rows collectively define one of multiple leadframes arranged in a matrix or a grid-like pattern. Along these lines, the semiconductor dies 20 and wires 24 used to interconnect the dies 20 to the leads 18 of the corresponding leadframe may all be covered by a single mold cap which is ultimately cut or singulated to facilitate the formation of separate package bodies 26, and hence the individual semiconductor packages 10.

[0029] In accordance with an alternative embodiment of the present invention, the assembly process described above in relation to the semiconductor package 10 may be modified by patterning the metal layer in the same manner described above, except that no plating traces are included in the patterned metal layer. Due to the absence of such plating traces, the plating of those portions of the top surfaces of the leads 18 exposed within the openings 14 of the outer and inner rows alone or in combination with the portion of the top surface of the die pad 16 exposed within the central opening 14 is facilitated through the implementation of an electroless plating process. More particularly, the copper wire bond surfaces defined by the exposed portions of the top surfaces of the leads 18 are coated with thin gold by an immersion gold and auto-catalytic plating process. This immersion gold plating is an aqueous galvanic chemical reaction during which a small amount of the copper of each lead 18 (and optionally the die pad 16) is replaced with gold which is dissolved in the plating bath. Thus, gold is plated directly onto each of the leads 18 at a thickness of approximately 0.07 micrometers, in contrast to the electrolytic nickel/gold plating process described above which involves the initial plating of a nickel layer of approximately a 2.0 micrometer thickness, followed by the plating of a gold layer at approximately a 0.75 micrometer thickness. As will be recognized by those of ordinary skill

in the art, use of the immersion gold plating process as an alternative to the above-described electrolytic plating process also eliminates the need for the completion of the second chemical etching process described above since no plating traces are included in the patterned metal layer. Due to the lack of any need to form the plating traces when the direct immersion gold plating process is used in relation to the fabrication of the semiconductor package 10, the number and density of leads 18 which may be included in the semiconductor package 10, and hence the number of input/outputs of the semiconductor package 10, may be maximized. One preferred sequence of process flow steps involved in the immersion gold plating process is provided in the chart of Figure 6. Also included in Figure 6 is an identification of preferred chemicals or agents used in each of the process flow steps, and comments regarding various attributes of certain ones of these chemical/agents and the preferred duration of certain steps. The TCU-36 chemical identified in Figure 6 provides the preferred 0.07 micrometer gold thickness specified above, with the secondary autocatalytic/electroless gold reaction (facilitated by TMX-22) being optional. The total gold thickness may be tailored to the requirements of a particular semiconductor package.

[0030] In yet another alternative embodiment of the present invention, an electroless nickel-immersion gold plating process may be used as an alternative to the above-described immersion gold plating process. In this process, the copper wire bond surfaces defined by the exposed portions of the top surfaces of the leads 18 are coated with thin nickel through the completion of an electroless nickel plating process which requires no outside source of electrons. This nickel plating process takes place through a chemical reduction process. Subsequent to the completion of the electroless nickel plating process, a gold plating process, and more particularly an immersion gold plating process similar to that described above but employing a different immersion gold chemistry, is completed. In this regard, the completion of the immersion gold plating on the electroless nickel takes place through a replacement reaction, again without any external source of electrons.

[0031] Referring now to Figures 3 and 4, there is shown a semiconductor package 30 constructed in accordance with a second embodiment of the present invention. The semiconductor package 30 comprises a film layer 32 which defines opposed, generally planar top and bottom surfaces. The film layer 32 is a generally planar sheet preferably fabricated from the same non-conductive material described above in relation to the film layer 12. Disposed within

the film layer 32 are a plurality of openings 34 which extend between the top and bottom surfaces thereof. Each of the openings 34 has a generally quadrangular (i.e., square) configuration. The openings 34 of the film layer 32 include a relatively large, generally square opening positioned in the approximate center of the film layer 32, and a series of smaller, generally square openings 34 which are arranged in an inner row which circumvents the central opening 34, and an outer row which circumvents the inner row. The openings 34 of the outer row extend to at least one of the peripheral edge segments of the film layer 32.

[0032] In addition to the film layer 32, the semiconductor package 30 includes a die pad 36 which itself defines opposed, generally planar top and bottom surfaces, and has a generally quadrangular (i.e., square) configuration. As seen in Figure 3, the peripheral portion of the bottom surface of the die pad 34 is attached to the top surface of the film layer 12 such that a substantial portion of the bottom surface of the die pad 36 is exposed within the central opening 34 of the film layer 32. The semiconductor package 30 also includes a plurality of leads 38 which each have a quadrangular configuration. Each lead 38 defines opposed, generally planar top and bottom surfaces. Additionally, the peripheral portion of the bottom surface of each lead 38 is attached to the top surface of the film layer 32 such that a substantial portion of the bottom surface of each lead 38 is exposed within a respective one of the openings 34 of the film layer 32 which are arranged in the inner and outer rows circumventing the central opening 34 (in which the die pad 36 is exposed). Thus, the leads 38 are themselves arranged in an inner row which circumvents the die pad 36 and an outer row which circumvents the inner row. The leads 38 of the outer row, like the openings 34 of the outer row, extend to at least one of the peripheral edge segments of the film layer 12. More particularly, those leads 38 (and openings 34) which are located at respected ones of the four corner regions defined by the film layer 32 extend to each of an adjacent pair of peripheral edge segments thereof. Those of ordinary skill in the art will recognize that the openings 34 of the inner and outer rows and the leads 38 may each have a configuration other than for a quadrangular or square configuration, e.g., a circular or other configuration.

[0033] The semiconductor package 30 further comprises an integrated circuit device or semiconductor die 40 which is attached to the top surface of the die pad 36. The attachment of the semiconductor die 40 to the die pad 36 is preferably accomplished through the use of a layer 42 of a suitable adhesive. The contacts or terminals of the semiconductor die 40 are electrically

connected to the top surfaces of respective ones of the leads 38 through the use of elongate, conductive bond wires 44. More particularly, each wire 44 has a first end which is electrically connected to a respective one of the pads or terminals of the semiconductor die 40, and an opposed, distal end which is electrically connected to the top surface of a respective one of the leads 38.

[0034] In the semiconductor package 30, the semiconductor die 40, wires 44, the top surfaces of the die pad 36 and leads 38, and portions of the top surface of the film layer 32 are covered by a package body 46 of the semiconductor package 30. The package body 46 has a generally square configuration, and defines a generally planar top surface and four generally planar side surfaces. The bottom surface of the package body 46 is completely covered by the combination of the film layer 32, die pad 36, and leads 38. The package body 46 is fabricated from the same material and by the same process described above in relation to the package body 26. In the completed semiconductor package 30, bottom surfaces of the die pad 36 and leads 38 extend in generally co-planar relation to each other along a plane which is generally parallel to and spaced inwardly from the plane defined by the bottom surface of the film layer 32. The leads 38 of the outer row each include an outer end which extends to and is substantially flush with a respective side surface of the package body 46.

[0035] As indicated above, in the semiconductor package 30, those portions of the bottom surfaces of the die pad 36 and leads 38 which are exposed within the openings 34 are recessed inwardly relative to the outer, bottom surface of the film layer 32. Thus, in order to facilitate the electrical connection of the semiconductor package 30 to an underlying substrate such as a printed circuit board (PCB), solder bumps 48 are preferably applied to the exposed portions of the bottom surfaces of the die pad 36 and leads 38. As seen in Figure 3, the solder bumps 48 are each preferably sized and configured to protrude slightly downwardly beyond the bottom surface of the film layer 32.

[0036] The manufacturing process associated with the semiconductor package 30 is substantially identical to that described above in relation to the semiconductor package 10 of the first embodiment. In the fabrication of the semiconductor package 30, either the above described electrolytic plating process or the electrodeless immersion gold plating process may be implemented to plate the top surfaces of the leads 38 and, optionally, the top surface of the die pad 36. However, in fabricating the semiconductor package 30, it is also contemplated that the

plating process will also be completed on those portions of the bottom surfaces of the die pad 36 and leads 38 which are exposed within respective ones of the openings 34. The completion of the plating process on such surfaces is used to provide more effective adhesion of the solder bumps 48 to the leads 38 and die pad 36. A further variation between the manufacturing process for the semiconductor package 30 and the semiconductor package 10 involves the formation of the solder bumps 48 upon the exposed portions of the bottom surfaces of the leads 38 and die pad 36, the solder bumps 48 preferably being formed subsequent to the formation of the package body 46.

[0037] Those of ordinary skill in the art will further recognize that multiple semiconductor packages 30 constructed in accordance with the second embodiment of the present invention may also be simultaneously fabricated by patterning a single metal layer to define multiple leadframes arranged in a matrix or grid-like pattern, as described above in relation to the semiconductor package 10. These individual leadframes may be effectively separated from each other through the implementation of a cutting or singulation operation subsequent to the formation of the solder bumps. The completion of the singulation process effectively separates the leadframes from each other, thus facilitating the creation of the individual semiconductor packages 30.

[0038] Referring now to Figure 5, there is shown a semiconductor package 50 constructed in accordance with a third embodiment of the present invention. The semiconductor package 50 has the same basic structural attributes of the metal face-out semiconductor package 10 of the first embodiment. In this regard, the semiconductor package 50 includes leads 52 which are arranged in an inner row circumventing die pad 54 of the semiconductor package 50, and an outer row which circumvents the inner row. However, in contrast to the arrangement of the leads 18 in the semiconductor package 10, the leads 52 of the outer row in the semiconductor package 50 are staggered or offset relative to the leads 52 of the inner row. Additionally, the semiconductor package 50 further includes an isolated ring structure 56 which circumvents the die pad 34, and extends between the peripheral edge of the die pad 54 and the leads 52 of the inner row. As will be recognized by those of ordinary skill in the art, the patterning of the metal layer and non-conductive sheet in the semiconductor package 50 is completed in a manner which facilitates the formation of the die pad 54, leads 52 and ring structure 56, and corresponding openings in the film layer of the semiconductor package 50 as is needed to allow for the

advancement of the bond wires to the leads 52, ring structure 56 and, optionally, the die pad 54. Those of ordinary skill in the art will further recognize that the structural attributes of the metal face-in semiconductor package 30 of the second embodiment may be modified to mirror those of the semiconductor package 50. Additionally, the semiconductor packages 10, 30 may each be modified to include the ring structure 56 of the semiconductor package 50. Further, though the semiconductor packages 10, 30 and 50 are each shown as including inner and outer rows of leads, those of ordinary skill in the art will recognize that fewer or greater than two rows of leads may be included in each such semiconductor package. The manufacturing methodology for the semiconductor package 50 substantially mirrors those described above in relation to the semiconductor packages 10, 30.

[0039] This disclosure provides exemplary embodiments for the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art and view of this disclosure.